WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell which stores a plurality of data with an n-valued threshold voltage (n is a natural number equal to or larger than 1);

a first data storage circuit which stores at least a first-logic-level or a second-logic-level data read from the memory cell;

a second data storage circuit which is connected to a data line and stores at least the first- or second-logic-level data supplied from the data line;

a third data storage circuit which stores at least the data read from the memory cell or the first- or second-logic-level data supplied from the first data storage circuit; and

a control circuit which manipulates the data in the first, second and third data storage circuits in such a manner that the control circuit does not change the threshold voltage of the memory cell when the logic level of the first data storage circuit is at the second logic level, carries out a first write operation to raise the threshold voltage of the memory cell when the logic level of the first data storage circuit is at the first logic level and the logic level of the third data storage circuit is at the first logic level, and carries out a second write operation to raise the threshold voltage of the memory cell when the logic

level of the third data storage circuit is at the second logic level,

which, in a first verify operation, does not precharge the memory cell when the logic level of the second data storage circuit is at the first logic level and precharges the memory cell when the logic level of the second data storage circuit is at the second logic level,

which sets the logic level of the third data storage circuit to the second logic level when the threshold voltage of the memory cell has exceeded a first verify voltage, does not change the logic level of the third data storage circuit when the threshold voltage of the memory cell has not exceeded the first verify voltage, sets the logic level of the first data storage circuit to the second logic level when the threshold voltage of the memory cell has exceeded a second verify voltage higher than the first verify voltage, and does not change the logic level of the first data storage circuit when the threshold voltage of the memory cell has not exceeded the second verify voltage,

which, in a second verify operation, does not precharge the memory cell when the logic level of the third data storage circuit is at the first logic level and precharges the memory cell when the logic level of the second data storage circuit is at the second logic

level,

which sets the logic level of the first data storage circuit to the second logic level when the threshold voltage of the memory cell has exceeded a third verify voltage higher than the second verify voltage, and does not change the logic level of the first data storage circuit when the threshold voltage of the memory cell has not exceeded the third verify voltage, and

which, in a third verify operation, sets the logic level of the first data storage circuit to the second logic level when the threshold voltage of the memory cell has exceeded a fourth verify voltage higher than the third verify voltage, does not change the logic level of the first data storage circuit when the threshold voltage of the memory cell has not exceeded the fourth verify voltage, and repeats the first and second write operations and verify operations until the logic level of the first data storage circuit reaches the second logic level.

2. The device according to claim 1, wherein the memory cell is composed of an EEPROM.

3. The device according to claim 1, wherein the memory cell constitutes a NAND flash memory.

4. The device according to claim 1, wherein the second write operation is slower in write speed than the first write operation.

5. A semiconductor memory device comprising:

a memory cell which store a plurality of data with an n-valued threshold voltage (n is a natural number equal to or larger than 1);

a first data storage circuit which stores at least a first-logic-level or a second-logic-level data read from the memory cell;

a second data storage circuit which is connected to a data line and stores at least the first- or second-logic-level data supplied from the data line;

a third data storage circuit which stores at least the data read from the memory cell or the first- or second-logic-level data supplied from the first data storage circuit; and

a control circuit which, after writing the data in a first page into the memory cell, stores the data in a second page via a data line into the second data storage circuit, stores the data in the first page read from the memory cell into the first data storage circuit, and manipulates the first, second, and third storage circuits in such a manner that the control circuit sets the second logic level in the third data storage circuit in a case where data "2" has been written into the memory cell or a case data "1" has been written into the memory cell and a first verify voltage has been exceeded, and, in other cases, sets the first logic level in the third data storage circuit.

6. The device according to claim 5, wherein the memory cell is composed of an EEPROM.

7. The device according to claim 5, wherein the memory cell constitutes a NAND flash memory.

8. A semiconductor memory device comprising:

a memory cell which stores a plurality of data with an n-valued threshold voltage (n is a natural number equal to or larger than 1);

a first data storage circuit which stores at least a first-logic-level or a second-logic-level data read from the memory cell;

a second data storage circuit which is connected to a data line and stores at least the first- or second-logic-level data supplied from the data line;

a third data storage circuit which stores at least the data read from the memory cell or the first- or second-logic-level data supplied from the first data storage circuit; and

a control circuit which stores the data in a first page supplied from the data line into the second data storage circuit, transfers the data in the first page stored in the second data storage circuit to the first data storage circuit, stores the data in a second page supplied from the data line into the second data storage circuit, sets write data on the basis of the data in the first page stored in the first data storage circuit and the data in the second page stored in the

second data storage circuit, and writes the data in the first page and the data in the second page into the memory cell at the same time on the basis of the write data.

9. The device according to claim 8, wherein the memory cell is composed of an EEPROM.

10. The device according to claim 8, wherein the memory cell constitutes a NAND flash memory.

11. A semiconductor memory device comprising:

a plurality of memory cells each of which is capable of having at least one of a first, a second, a third, and a fourth threshold voltage and stores two bits of data; and

a write circuit which controls the threshold voltages of said plurality of memory cells to write data and which includes

a first step of, according to data to be written, keeping the threshold voltage of a first memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the third threshold voltage,

a second step of, according to data to be written, keeping the threshold voltage of a second memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the third threshold voltage, and

a third step of, when the threshold voltage

of the first memory cell is the first threshold voltage, according to data to be written, keeping the threshold voltage of the first memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the second threshold voltage, and of, when the threshold voltage of the first memory cell is the third threshold voltage, according to data to be written, keeping the threshold voltage of the first memory cell at the third threshold voltage or changing the threshold voltage from the third threshold voltage to the fourth threshold voltage, and

which, when the threshold voltage of the first memory cell is kept at the third threshold voltage in the third step, changes the threshold voltage of the first memory cell if the threshold voltage of the first memory cell has not reached a specific threshold voltage.

12. The device according to claim 11, wherein the second threshold voltage lies between the first threshold voltage and the third threshold voltage.

13. The device according to claim 12, wherein each of the second threshold voltage and the third threshold voltage lies between the first threshold voltage and the fourth threshold voltage.

14. The device according to claim 11, wherein the write circuit further includes

a fourth step of, when the threshold voltage of

the second memory cell is the first threshold voltage, according to data to be written, keeping the threshold voltage of the second memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the second threshold voltage, and of, when the threshold voltage of the second memory cell is the third threshold voltage, according to data to be written, keeping the threshold voltage of the second memory cell at the third threshold voltage or changing the threshold voltage from the third threshold voltage to the fourth threshold voltage.

15. The device according to claim 14, wherein the write circuit changes the threshold voltage of the second memory cell, if the threshold voltage of the second memory cell has not reached a specific threshold voltage in the fourth step of keeping the threshold voltage of the second memory cell at the third threshold voltage.

16. The device according to claim 11, wherein the first memory cell and the second memory cell are provided so as to be adjacent to each other.

17. The device according to claim 11, wherein the first memory cell and the second memory cell are connected to a common word line and provided so as to be adjacent to each other.

18. The device according to claim 11, wherein the

first memory cell and the second memory cell are connected to a common bit line and provided so as to be adjacent to each other.

19. The device according to claim 11, wherein the definition of the value of the third threshold voltage before the third step differs from that after the third step.

20. The device according to claim 19, further comprising a third memory cell which stores data that indicates whether the third step has been carried out or not, in order to control the value of the third threshold voltage.

21. A semiconductor memory device comprising:

a plurality of memory cells each of which is capable of having at least one of a first, a second, a third, and a fourth threshold voltage and stores two bits of data; and

a write circuit which controls the threshold voltages of said plurality of memory cells to write data and which includes

a first step of, according to data to be written, keeping the threshold voltage of a first memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the third threshold voltage,

a second step of, according to data to be written, keeping the threshold voltage of a second

memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the third threshold voltage,

a third step of, according to data to be written, keeping the threshold voltage of a third memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the third threshold voltage, and

a fourth step of, when the threshold voltage of the first memory cell is the first threshold voltage, according to data to be written, keeping the threshold voltage of the first memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the second threshold voltage, and of, when the threshold voltage of the first memory cell is the third threshold voltage, according to data to be written, keeping the threshold voltage of the first memory cell at the third threshold voltage or changing the threshold voltage from the third threshold voltage to the fourth threshold voltage.

22. The device according to claim 21, wherein the write circuit changes the threshold voltage of the first memory cell, when the threshold voltage of the first memory cell has not reached a specific threshold voltage in the fourth step of keeping the threshold voltage of the first memory cell at the third threshold voltage.

23. The device according to claim 21, wherein the second threshold voltage lies between the first threshold voltage and the third threshold voltage.

24. The device according to claim 23, wherein each of the second threshold voltage and the third threshold voltage lies between the first threshold voltage and the fourth threshold voltage.

25. The device according to claim 22, wherein the write circuit further includes

a fifth step of, when the threshold voltage is the first threshold voltage, according to data to be written, keeping the threshold voltages of the second memory cell and the third memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the second threshold voltage, and of, when the threshold voltage is the third threshold voltage, according to data to be written, keeping the threshold voltages of the second memory cell and the third memory cell at the third threshold voltage or changing the threshold voltage from the third threshold voltage to the fourth threshold voltage.

26. The device according to claim 25, wherein the write circuit changes the threshold voltages of the second memory cell and the third memory cell, when the threshold voltages of the second memory cell and the third memory cell have not reached a specific threshold

voltage in the fifth step of keeping the threshold voltages at the third threshold voltage.

27. The device according to claim 21, wherein the first memory cell and the second memory cell are provided so as to be adjacent to each other and the first memory cell and the third memory cell are provided so as to be adjacent to each other.

28. The device according to claim 21, wherein the first memory cell and the second memory cell are connected to a common word line and provided so as to be adjacent to each other and the first memory cell and the third memory cell are connected to a common bit line and provided so as to be adjacent to each other.

29. The device according to claim 22, wherein the definition of the value of the third threshold voltage before the fourth step differs from that after the fourth step.

30. The device according to claim 29, further comprising a fourth memory cell which stores data that indicates whether the fourth step has been carried out or not, in order to control the value of the third threshold voltage.